Application No. 09/630,258
Filed: August 1, 2000
TC Art Unit: 2124
Confirmation No.: 7200

AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of computing a fast Fourier transform in a plurality of computation stages, the method comprising:

(a) receiving N time-ordered first data values;

(b) sequentially storing in a first memory each of said N time-ordered first data values in the time-order;

(c) storing in a second memory a plurality of twiddle factors in a bit reversed order;

(d) reading a predetermined number R of input butterfly data values of said N first data values, wherein said predetermined number R of input butterfly data values are separated by N/R first data values in said N time-ordered first data values;

(e) performing a radix R butterfly calculation on said predetermined number R of input butterfly ~~input~~ data values using at least one of the plurality of twiddle factors stored in the second memory to generate R output butterfly ~~output~~ data values;

(f) storing said R output butterfly ~~output~~ data values in sequential memory locations of a third memory; and

(g) performing said steps (c) - (f) N/R x 2 times, wherein the predetermined number R is the same predetermined number each time the steps (d) - (f) are performed,

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wherein said reading step (d) includes reading the R output butterfly data values from said third memory, ~~and~~

wherein the memory store operation performed in said storing step (f) has a unity stride, thereby allowing R output butterfly data values to be read from contiguous memory locations each time the R output butterfly data values are read from said third memory, and

wherein said steps (a) - (g) are performed in each one of the plurality of computation stages.

2. (currently amended) The method as in claim 1 further comprising the steps of:

replacing said N first data values in said first memory with selected ones of said R output butterfly ~~output~~ data values stored in said third memory location;

repeating steps (c) - (g) a total of $\log_r(n)$ times.

3. (currently amended) The method as in claim 1, wherein said predetermined number R[=] equals 2.

4. (currently amended) The method as in claim 1, wherein said predetermined number R[=] equals 4.

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5. (currently amended) Apparatus for calculating a fast Fourier transform, the apparatus comprising:

a plurality of computation stages, each computation stage comprising

a first processor stage having an output including

a first memory storing N time-ordered ~~input~~ first data values, said N ~~input~~ first data values being stored in said first memory sequentially in the time-order,

a second memory storing a plurality of twiddle factor values, said plurality of twiddle factor values being stored in said second memory in a bit-reversed order,

a third memory storing a plurality of output butterfly data values, and

a ~~radix R~~ fast Fourier transform calculator coupled to said first, second, and third memories, said ~~radix R~~ fast Fourier transform calculator being operative

to receive a predetermined number R of selected input butterfly data values of said N ~~input~~ first data values, the predetermined number R of input butterfly data values being separated by N/R ~~input~~ first data values, ~~said radix R fast Fourier transform calculator being further operative to~~

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to receive at least one twiddle factor value from said second memory, ~~and said radix R fast Fourier transform calculator being further operative~~

to perform a radix R butterfly calculation to calculate R output butterfly data values using the at least one twiddle factor value, ~~and~~

to write said R output butterfly data values into sequential memory locations of said third memory, and

to perform said second receiving operation, said first performing operation, and said writing operation N/R x 2 times, wherein the predetermined number R is the same predetermined number each time the second receiving, the first performing, and the writing operations are performed~~;~~, and

a second processor stage coupled to said output of said first processor stage,

wherein calculations performed in said second processing stage include reading the R output butterfly data values from said third memory, and

wherein the memory write operation performed by said ~~radix R~~ fast Fourier transform calculator into the sequential memory locations of said third memory has a unity stride, thereby allowing R output butterfly data values to be read from contiguous

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memory each time the R output butterfly data values are read from said third memory.

6. (currently amended) The apparatus of claim 5 wherein the predetermined number R equals 2.

7. (currently amended) The apparatus of claim 5 wherein the predetermined number R equals 4.

8. (currently amended) Digital signal processing apparatus for performing a fast Fourier transform calculation, comprising:

a plurality of computation stages, each computation stage comprising

a first processor stage having an output and including

a digital signal processor operative

to receive N time-ordered first data values,

~~said digital signal processor operative~~ to sequentially store in a first memory each of said N first data values in the time-order,

~~said digital signal processor operative~~ to store in a second memory a plurality of twiddle factors in a bit reversed order~~;~~,

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~~said digital signal processor operative~~ to read a predetermined number R of input butterfly data values of said N first data values, wherein said predetermined number R of input butterfly data values are separated by N/R data points in said N time-ordered first data values,

~~said digital signal processor operative~~ to perform a radix R butterfly calculation on said predetermined number R of input butterfly ~~input~~ data values,

~~said digital signal processor operative~~ to provide R output butterfly ~~output~~ data values using at least one of said plurality of twiddle factors, ~~and~~

~~said digital signal processor operative~~ to sequentially store said R output butterfly ~~output~~ data values in sequential memory locations of a third memory, and

to perform said first storing operation, said reading operation, said first performing operation, said providing operation, and said second storing operation N/R x 2 times, wherein the predetermined number R is the same predetermined number each time the first storing, the reading, the first performing, the providing, and the second storing operations are performed~~;~~, and

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a second processor stage having an input coupled to said output of said first processor stage,

wherein calculations performed in said second processor stage include reading the R output butterfly data values from said third memory, and

wherein the memory store operation performed by said digital signal processor in the sequential memory locations of said third memory has a unity stride, thereby allowing R output butterfly data values to be read from contiguous memory locations each time the R output butterfly data values are read from said third memory.

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